

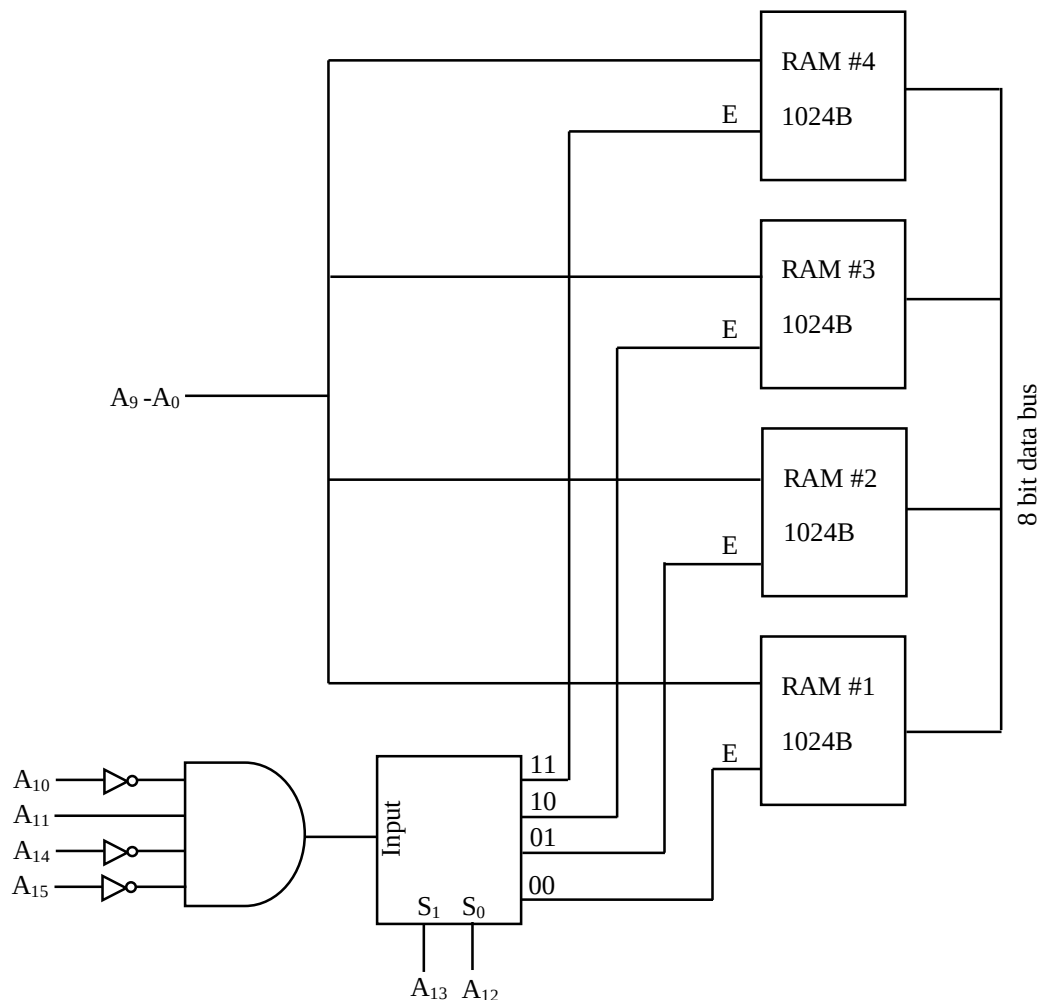
Semiconductor Memories

ONE-MARK QUESTIONS

- 11.1 In a DRAM information is stored in a capacitor. So, option 'b' is correct.
- 11.2 Each cell of a static Random Access Memory contains 6 MOS transistors. So, option 'a' is correct.
- 11.3 Each cell of a static Random Access Memory contains 1 transistor and 1 capacitor. So, option 'b' is correct.

TWO-MARKS QUESTIONS

11.1



The output of AND gate is used to enable the 2:4 decoder. So, the AND gate output must be high. Each memory has 1kB capacity. So, within each memory address will range from 000 to 3FF. Further, one of the memory chips is selected using decoder output which is dependent on A_{13} and A_{12} . From all these requirements we can write

			S ₁	S ₀				Address Type	RAM Block #	Address in Hex
A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈			
0	0	0	0	1	0	0	0	Start Address	1	08FF
0	0	0	0	1	0	1	1	End Address		0BFF
0	0	0	1	1	0	0	0	Start Address	2	1800
0	0	0	1	1	0	1	1	End Address		1BFF
0	0	1	0	1	0	0	0	Start Address	3	2800
0	0	1	0	1	0	1	1	End Address		2BFF
0	0	1	1	1	0	0	0	Start Address	4	3800
0	0	1	1	1	0	1	1	End Address		3BFF

So, option 'd' is correct.

11.2 Address lines A₀ to A₇ are required in both chips and A₁₀ to A₁₅ are not used either of the chips.

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	Address Type	Chip No
x	x	x	x	x	x	0	1	Start Address	1
x	x	x	x	x	x	0	1	End Address	
x	x	x	x	x	x	1	0	Start Address	2
x	x	x	x	x	x	1	0	End Address	

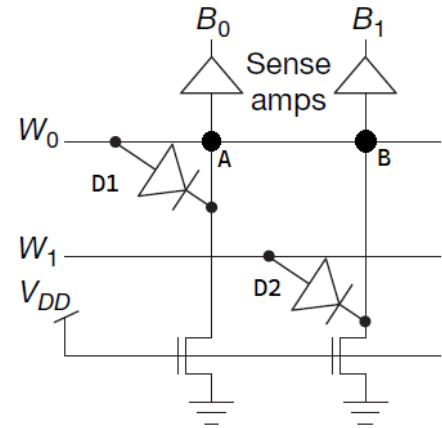
Since A₁₅ to A₁₀ address lines can have any combination of 1s and 0's, addresses 0100, 1500 and F900 may fall in Chip 1. So, option 'a' 'b' and 'c' are incorrect. However, address F800-F900 is not falling any of the chips. So, option 'd' is correct.

11.3 There are two NMOS devices in this ROM array. Their gate terminals are connected to supply voltage V_{DD} and source terminals are at the ground potential. Therefore, both devices are conducting and V_{DS} will be close to zero. It means potential at cathode terminal of diodes is almost negligible.

It is stated that at a time one word line goes high and the other is in high impedance state. So, when W₀ is high, diode D₁ it will get forward biased which will be sensed by the sense amplifier and B₀ = 1. But at this time W₁ is in high impedance state. So, diode D₂ will be OFF and B₁ = 0.

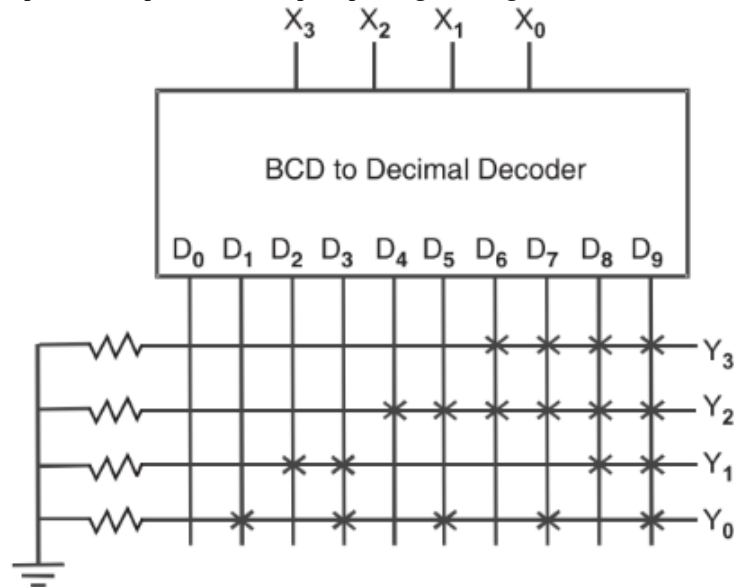
Similarly, when W₁ is high, diode D₂ it will be forward biased which will be sensed by the sense amplifier and B₁ = 1. But at this time W₀ is in high impedance state. So, diode D₁ will be OFF and B₀ = 0.

Now writing this in the given matrix form,
So, option 'a' is correct.



$$\begin{bmatrix} D_{00} & D_{01} \\ D_{10} & D_{11} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

11.4 Let's write input and output relationship inspecting the diagram



Decimal input	X ₃	X ₂	X ₁	X ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	1	1	0	0
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

It is clear from this table that it is neither a gray code nor an excess-3 code converter. So, checking possibility of 2-4-2-1 BCD numbers. It is clear by inspection that up to number 5, it is satisfying 2-4-2-1 BCD numbers. So, testing for left of the numbers.

Weightage	8	4	2	1	2	4	2	1	
Decimal input	X ₃	X ₂	X ₁	X ₀	Y ₃	Y ₂	Y ₁	Y ₀	Output in decimal
6	0	1	1	0	1	1	0	0	6
7	0	1	1	1	1	1	0	1	7
8	1	0	0	0	1	1	1	0	8
9	1	0	0	1	1	1	1	1	9

It is satisfying 2-4-2-1 BCD numbers requirement. So, it is a 2-4-2-1 BCD number converter and 'b' is the correct option.